REMARKS

Objected to claims 10, 11, 13 and 21 have been amended to overcome the objection thereto and claim 12 has been amended to depend from objected to claim 11. Claims 1 to 21 remain active in this application of which claims 14 and 15 have been allowed and claims 10, 11, 13 and 21 have been indicated to be allowable. Please charge any costs to Deposit Account No. 20-0668.

Claims 1 to 4, 9, 12, 16, 17 and 20 were rejected under 35 U.S.C. 102(e as being anticipated by Gilhousen et al. (U.S. 5,715,236). The rejection is again respectfully traversed for the same reasons as previously presented since there is still no showing on the record how the Examiner alleges the claims are anticipated by Gilhousen et al.

It is respectfully submitted that in rejecting claims as being anticipated under section 102, it is incumbent upon the Examiner to initially establish a prima facie case of anticipation. This requires that each and every structural feature and its function as well as each method step and its function be clearly shown to be present in a single reference. As is apparent, this has not been done and, accordingly, no prima facie case of obviousness has been presented. If the rejection is to be sustained, it is necessary that the Examiner show, on the record, how the claims are readable on Gilhousen et al. Without such showing, applicants are unable to determine how to respond to the rejection without clairvoyance.

More specifically, claim 1 requires a receive input for receiving a CDMA encoded signal. The Office action fails to show what structure of Gilhousen et al. meets this limitation. There are many possible inputs in Figure 2 of Gilhousen et al.

Claim 1 further requires a multiply/accumulate device for multiplying the received signal received on the receive input by the predetermined CDMA code word and operating in the analog domain, the multiply/accumulate device operable to accumulate the results of the multiplication operation over a symbol period to provide an analog result. The Office action fails to show what structure of Gilhousen et al. meets this limitation.

Claim 1 still further requires a data conversion device for determining if the analog result corresponds to a predetermined digital state and, if so, generating a digital output corresponding to the predetermined digital state. The Office action fails to show what structure of Gilhousen et al. meets this limitation.

Claim 2 further limits claim 1 by requiring that the predetermined digital state comprise multiple predetermined digital states and wherein the data conversion device is operable to generate multiple digital output states corresponding to the one of the multiple predetermined digital states to which the analog result has been determined to correspond. The Office action fails to show what structure of Gilhousen et al. meets this limitation.

Claim 3 further limits claim 2 by requiring that the multiple predetermined digital states correspond to a "+1" logic state, a "0" logic state and a "-1" state. The Office action fails to show what structure of Gilhousen et al. meets this limitation.

Claim 4 further limits claim 1 by requiring that the data conversion device, by the operation of generating the digital output, provide a correlation of the encoded signal with the generated code word for the associated ACDMA channel. The Office action fails to show what structure of Gilhousen et al. meets this limitation.

Claim 9 further limits claim 1 by requiring that the code generator be operable to generate a plurality of CDMA codes, each associated with one of a plurality of CDMA channels such that the received input can receive a plurality of CDMA encoded signals each on a different channel and further comprising a plurality of multiply/accumulate devices, one for each channel and for each code word generated by the code generator and wherein the data conversion device is operable to determine for each of the multiply/accumulation devices if the associated analog result corresponds to the predetermined digital state and if so, generating a digital output corresponding to the associated multiply/accumulation device such that a digital output is provided for each of the multiply/accumulation devices. The Office action fails to show what structure of Gilhousen et al. meets this limitation.

Claim 12 further limits claim 1 by requiring an automatic gain control device for adjusting the gain of each of the multiply/accumulation device. While this feature is shown in Gilhousen et al., there is no showing that the combination as claimed is shown in Gilhousen et al. as required by In re Beaver, 893 F.2d 329, 330, 13 USPQ2d 1409, 1410 (Fed. Cir. 1989).

Claim 16 requires the step of receiving the CDMA encoded signal on a receive input. The Office action fails to show where in Gilhousen et al. this limitation is found.

Claim 16 further requires the step of multiplying the received signal received on the receive input by the predetermined CDMA code word in the analog domain and accumulating the result of the multiplication operation over a symbol period to provide an analog result. The Office action fails to show where in Gilhousen et al. this limitation is found.

Claim 16 still further requires the step of determining if the analog result corresponds to a predetermined digital state and, if so, generating a digital output corresponding to the predetermined digital state. The Office action fails to show where in Gilhousen et al. this limitation is found.

Claim 17 limits claim 16 by requiring that the predetermined digital state comprise multiple predetermined digital states, and wherein the step of generating a digital output is operable to generate multiple digital output states, each corresponding to the one of the multiple predetermined digital states to which the analog result has been determined to correspond. The Office action fails to show where in Gilhousen et al. this limitation is found.

Claim 20 limits claim 16 by requiring that the step of generating the predetermined CDMA code be operable to generate a plurality of CDMA codes, each associated with one of a plurality of CDMA channels such that the receive input can receive a plurality of CDMA encoded signals each on a different channel and further comprising the step of providing a plurality of multiply/accumulation devices, each for carrying out the multiplying and accumulation steps for a given one of the CDMA channels and wherein the step of determining for each of the multiply/accumulation devices is operable to determine if the associated analog result corresponds to the predetermined digital state and, if so, generating a digital output corresponding to the associated multiply/accumulation device such that a digital output is provide for each of the multiply/accumulation devices. The Office action fails to show where in Gilhousen et al. this limitation is found.

Claims 5 to 8, 18 and 19 were rejected under 35 U.S.C. 103(a) as being unpatentable over Gilhousen et al. in view of Hendrickson et al. (U.S. 5,974,584). The rejection is respectfully traversed.

The argument presented above with reference to the rejection under 35 U.S.C. 102(e) applies as well to these claims.

More specifically, claims 5 to 8 depend from claim 1 and, accordingly, the arguments presented above with reference to claim 1 apply since Hendrickson et al. and the discussion relative to Hendrickson et al. fails to overcome the deficiencies in the rejection of claim 1 as noted above.

In addition, claim 5 further limits claim 1 by requiring that the code generator operate in synchronization with a chip clock such that the predetermined CDMA code word is clocked by the chip clock, which chip clock changes from one logic state to a second logic state, and the multiply/accumulation device further includes a blanking device for blanking the operation of the multiply/accumulation device during at least one of the leading or lagging edges of the chip clock at the one logic state for a predetermined blanking duration during which the operation of the multiply/accumulation device is inhibited to prevent accumulation of information therefrom. No such structure has been shown to be contained in Gilhousen et al., Hendrickson et al. or any proper combination of these references.

Claim 6 further limits claim 5 by requiring that the blanking device operate during the leading and lagging edges of the chip clock. No such structure has been shown to be contained in Gilhousen et al., Hendrickson et al. or any proper combination of these references.

Claim 7 further limits claim 1 by requiring a blanking device for blanking the operation of the multiply/accumulation device for at least one of the leading or the lagging edges of the received signal for a predetermined blanking duration when transitioning between logic states. No such structure has been shown to be contained in Gilhousen et al., Hendrickson et al. or any proper combination of these references.

Claim 8 further limits claim 7 by requiring that the blanking device be operable to blank the operation of the multiply/accumulation device for both the leading and lagging edges for the predetermined blanking duration. No such structure has been shown to be contained in Gilhousen et al., Hendrickson et al. or any proper combination of these references.

Claim 18 further limits claim 16 by requiring that the step of generating the code word be operable to generate a sequence of logic states that are synchronized with a chip clock such that the predetermined CDMA code word is comprised of a plurality of logic states that are clocked by the chip clock, which chip clock changes from one logic state to a second logic state and the step of multiplying and the step of accumulating further including the step of blanking the operation of multiplying and accumulating during at least one of the leading or lagging edges of the chip clock at the one logic state for a predetermined blanking duration during which the multiplying and accumulation steps are inhibited to prevent accumulation of information therefrom. No such structure has been shown to be contained in Gilhousen et al., Hendrickson et al. or any proper combination of these references.

Claim 19 further limits claim 18 by requiring that the step of blanking operate only during the leading and lagging edges of the chip clock. No such structure has been

shown to be contained in Gilhousen et al., Hendrickson et al. or any proper combination of these references.

In view of the above remarks, favorable reconsideration and allowance are respectfully requested.

Respectfully submitted,

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